A Digitally Controlled Low Voltage Variable Gain Amplifier with Constant Return Loss

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***Abstract*—This paper presents a Variable Gain Amplifier operating at 4GHz with 1.2V of supply voltage and 250MHz bandwidth. The proposed configuration uses a mixture of voltage and current mode techniques to achieve a constant return loss, at both the input and the output, giving efficient power transmission completely independent of gain variations. SPECTRE simulations on the designed amplifier reveal a -12dB to 15dB gain variation in 3dB steps, with both S11 and S22 staying constant with a mean of –16.83dB and –21.37dB respectively. SPECTRE simulations also show a 1dB Power Compression point of -18.15dBm at the highest gain and a Power Gain variation of -10.73 to 16.17dB. The amplifier is also stable for all gain variations and is designed using a 90nm CMOS processes.**

***Index Terms*— CMOS, Noise Factor, Power Gain, Return Loss, RF Variable Gain Amplifier, VGA, Voltage Gain.**

I. Introduction

In wireless transmission, the signal strength between the transmitter and receiver depends upon many factors; the distance between the source and the receiver, condition of the channel and the path loss [1-3]. Therefore, the received signal is usually not constant, but rather varies depending on such factors. The Automatic Gain Control (AGC) block, deployed at the receiver end, plays an important role in ensuring that a constant amplitude signal is delivered to any subsequent stages for signal processing. Due to the rapid increase in the use of wireless communications systems, especially portable ones, the use of AGC blocks has consequently increased. The main part of the AGC block is the variable gain amplifier (VGA).

There are many different VGA topologies based on i) source degeneration [4], ii) transistor operating range variation [5], iii) current signal steering between the load and the supply voltage [6], iv) logarithmic gain control [7], v) gain control using a variable load [8] or vi) gain control using a variable linear resistor in the amplifier [9]. This paper describes a new simple VGA architecture, one which is based on a combination of current mode and voltage mode design to achieve constant return loss and good linearity while at the same time operating at a low voltage. Constant return loss ensures steady and efficient power transmission to and from the VGA.The VGA is designed to be used in a weaver receiver for WCDMA applications with 250MHz bandwidth. Section 2 describes the design of the amplifier and Section 3 provides the characteristics of the amplifier designed in a standard 90nm CMOS processes.

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II. VGA Design

A. System Level Implementation

The system Level Implementation of the proposed architecture is shown in Fig. 1. In the first Stage, the input voltage signal is converted to a current signal with the aid of a voltage to current converter. In the second stage, that converted current signal is varied using a digitally controlled current mode block. Finally, in the third stage the processed current signal is changed back to voltage mode.

The main benefit of using such architecture is that the gain is varied at an intermediate stage, rendering the input and the output stages isolated from any impact of gain variations. This ensures that the input and output stage have a constant biasing level for all gain changes, hence giving a constant return loss (S_{11}, S_{22}) at any gain. This further implies that a single impedance matching network, at the input and the output, can be designed for the frequency band of interest.

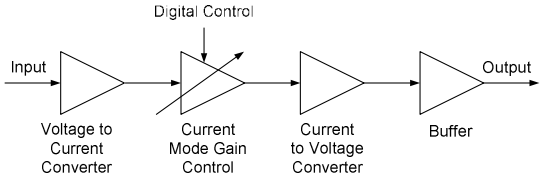

Fig. 1. System Level Implementation of the VGA

B. VGA Schematic

The complete transistor level diagram of the proposed VGA architecture is shown in Fig. 2. V_2, V_4, V_5, V_6, V_7 and V_8 are DC biasing voltages. These voltages are easily generated using an on chip constant g_m biasingcircuit.Measurement results in Section III indicate that using a constant g_m biasing circuit also minimizes the temperature and the process variations on the VGA operation.L_g and L_s are used for the input impedance matching network; whereas C_{o1}, C_{o2} and L_o make the output impedance matching network. An AGC circuit not shown controls all the switches.

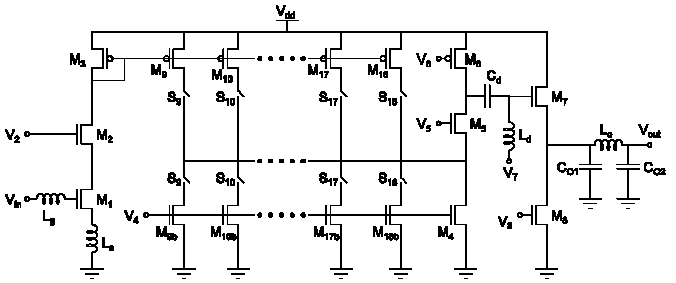

Fig. 2.Transistor Level Implementation of the Proposed VGA. Biasing Circuit and the Control Block Are Not Shown.

A simplified VGA circuit assuming one of the switches (S_9) is ON, is shown in Fig. 3. The DC and small signal AC currents in important branches are illustrated in the figure. The input signal is first converted to a current, by transistor M_1, which flows into M_3 through M_2. M_2 is required for better isolation.Transistor M_3 mirrors both the DC current and the small signal AC current to the other side.When switch S_9 is ON and other switches are OFF, M_9 and M_{9b} will be activated. M_{9b} is sized such that the entire DC current mirrored from M_3 and flowing into M_9 goes through it. Similarly, M_4 acts as a constant current source and biases M_5 and M_6 with a constant DC current.

Moreover, the small signal AC current mirrored from M_3 to M_9 divides between transistors M_{9b}, M_4 and M_5.Transistor M_5 acts as a common gate amplifier, and converts the small signal AC current that flows through it into AC voltage at node B.Transistors M_5 and M_6 are biased with a fixed DC current using $M_4$and therefore, the biasing voltages and small signal capacitors and resistorsassociated with node B remain constant.Finally, the AC voltage at node B is buffered to the output.

The ratio of M_9, M_{10}, M_{11}, …., M_{17} and M_{18}, with respect to M3 is such that different AC currents are mirrored towards node A to achieve different gains. Switches S_9, S_{10}, S_{11}, …., S_{17} and S_{18} are used to turn ON and OFF a particular branch at a given time.Subsequently,the size of M_{9b}, M_{10b},M_{11b},…, M_{17b} and M_{18b}transistors are selected to ensure the entire DC current from M_9, M_{10},M_{11}, …., M_{17} and M_{18} flows through them, respectively. This guarantees that M_5 and M_6 are always biased with a constant current generated by M_4.

The first branch in the circuit, composed of M_1, M_2 and M_3, and the finalbranch, consisting of M_4, M_5 and M_6,are driven with a constant DC current, generated by a g_m biasing circuit, to minimize the impact of temperature variation on the circuit performance. Therefore, DC voltages at the input, node B and the output remain constant along with small-signal parasitic capacitors and resistors. This gives a near constant return losses at both the input and the output for different gain changes.

The number of switches and current steering branches control the gain steps. Whereas, the ratio of the transistors M_9, M_{10}, M_{11}, …., M_{17} and M_{18} with respect to M_3, to a first order analysis, controls the gain at each step. Transistors are matched in the layout as much as possible to minimize the impact of process variation on the circuit performance.

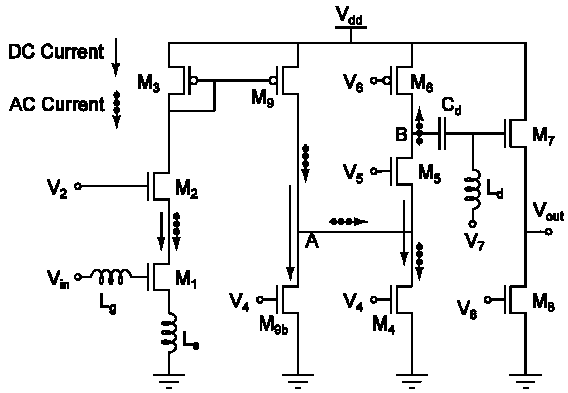

Fig. 3.Simplified VGA Assuming Switch S_9 is ON

The circuit, shown in Fig. 4, is used to generate biasing voltagesin the VGA. The circuit uses positive feedback and ensures the input and the output biasing currents only depend on the ratio of transistor sizes. Since process and temperature variations affect both transistors equally while their ratio remains the same, desired biasing currents can be generated.

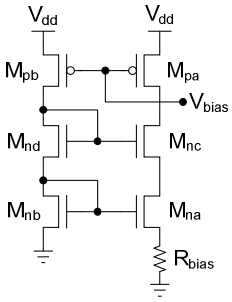

Fig. 4. The Constant g_m Biasing Circuit

C. Design Equations

The input of the VGA is a common source amplifier with inductive source degenerationto help with matching the real part of the impedance seen at the gate of $M_1$to the input port impedance of 50Ω.The gate inductor, Lg, is used to cancel the imaginary component of the impedance at the gate of M_1. The impedance matching network can approximately be designed using equations 1 and 2 [10].Since it is difficult to achieve low noise figure as well as good impedance matching simultaneously, transistor M_1 width was optimized, such that to obtain reasonable values of both the noise figure as well as input matching.

$$Z_{in} \approx \frac{g_{m1}}{C_{gs1}} \times L_s \quad (1)$$

$$\omega_o = \frac{1}{\sqrt{(L_g + L_s)C_{gs1}}} \quad (2)$$

The gain of the device can be calculated using the following equations and the simplified small signal model shown in Fig. 5.Thetransconductance of the input stage, consisting of M_1 and Ls,can be computed using

$$G_m = \frac{g_{m1}}{\omega_o C_{gs1}(R_s+\omega_T L_s)} \quad (3)$$

The small signal AC currentis given by

$$I_{AC} = G_m \times V_{in} \quad (4)$$

Assuming M_2 acts as a unity current buffer, the AC current in equation 4 is mirrored by the PMOS transistor M_3 to the current steering branch which is switched ON. This current is multiplied by the corresponding mirror ratio as shown in equation 5.

$$I_{mirror} = I_{AC} \times \frac{N}{W} \quad (5)$$

where W is the channel width of transistor M_3 and Nis the corresponding size of the mirror transistor M_9, M_{10}, M_{11}, …., M_{17} and M_{18}that is switched ON.

This mirrored AC current divides between the impedance seen down into node A, Z_{DA}, and the impedance seen at the source of M_5, Z_{UA}, shown in equation 6.

$$I_b = I_{mirror}\frac{Z_{DA}}{Z_{UA}+Z_{DA}} \quad (6)$$

where,

$$Z_{DA} \approx R_{DS4}||\frac{1}{sC_{dg4}}||R_{DS9,\ldots,DS18}||\frac{1}{sC_{dg9,\ldots,dg18}}||\frac{1}{sC_{gs5}} \quad (7)$$

$$Z_{UA} \approx \frac{1}{g_{m5}} \quad (8)$$

At node B the small signal AC gain can be calculated using equation 9.

$$V_b = I_b \times Z_b \quad (9)$$

where,

$$Z_b = (Z_6||Z_5||Z_{in7}) \quad (10)$$

The impedance seen at the gate of M_7, after neglecting the effects of $C_{gd7}$and C_{gd8}, is given by

$$Z_{in7} \approx (R_{ds8}||R_{ds7})\left(1+\frac{g_{m7}}{sC_{gs7}}+\frac{1}{sC_{gs7}(R_{ds8}||R_{ds7})}\right) \quad (11)$$

$$Z_5 \approx (g_{m5}Z_{DA}R_{ds5})||\frac{1}{sC_{dg5}} \quad (12)$$

$$Z_6 \approx R_{ds6}||\frac{1}{sC_{gd6}} \quad (13)$$

where, Z_5 and Z_6 are the impedances seen looking into the drain of M_5 and M_6, respectively.

Finally, the total gain at the output node in Fig. 3, combining the gain at node B with that of the buffer composed of M_7 and M_8, is given by

$$\frac{V_{out}}{V_{in}} \approx \frac{I_b Z_b(g_{m7}+sC_{gs7})}{s(C_{gd8}+C_{gs7})+g_{m7}} \quad (14)$$

These equationsare used to calculate the voltage gain approximately and extract W and N. The output impedance matching is also achieved using a pi- network composed of L_o, C_{o1}, and C_{o2}.

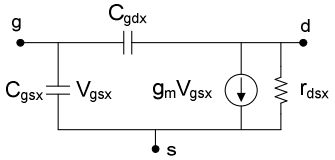

Fig. 5. Simplified Transistor Model Used for Small Signal Analysis

III. MEASUREMENT RESULTS

The VGA is designed using a 1.2V standard 90nm CMOS technology with 9 level of metallization. Only 3 metal layers are used for interconnects. Inductors are designed using top metal layer. The VGA is designed to match to 50Ω loads at input and output ports. All components are on-chip except L_d and C_d which are used for biasing and coupling, respectively.The layout of the VGA is shown in Fig. 6 and includes inductors $L_g$and L_o, capacitors $C_{o1}$and C_{o2} and Transistors used in the VGA. The source degeneration inductor L_s is small and is implemented using a wire inductor. Theoverall size of the layout including pads is 450µm by 220µm. The 10 gainstages are placed at the center of the design and occupy 120µm by 32µm of area. All designed inductors have patternground shield to maximize Quality Factor and minimize substrate losses. The achievedQuality Factorfor inductors, characterized by ADS momentum, is about 20. Pin V_3 is used to connect the external resistor to the constant g_m biasing circuit.

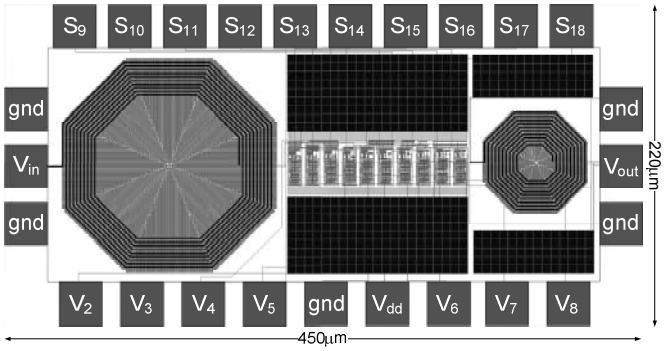

Fig. 6. The VGA Layout Including Bonding Pads

A. S-Parameter Responses

The S parameter responsesof the circuit are shown in Figs.7, 8 and9. As seen in Fig.7, S_{11}or the input return loss remains relatively constant, with a mean of -16.83dB and very small -0.3% to +0.12% variations for all process corners. The output return loss, S_{22}, is shown in Fig.8. S_{22} has a maximum variation of -2.3% to +1.03% from a mean of -21.37dB. Fig.9 shows S_{12} or the reverse isolation from the output to the

inputof the amplifier. The VGA considerably prevents reverse transmission,as seen in Fig. 9.

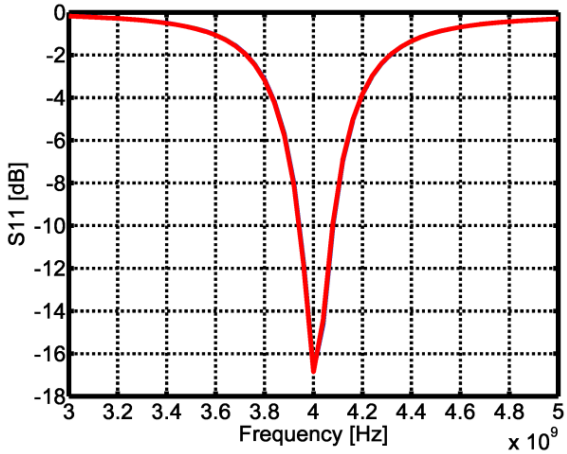

Fig. 7.The Input Return Loss (S_{11}) as a Function of Frequency. The input return loss always remains low at -16.83dB at 4GHz because of the constant biasing current at input stage.

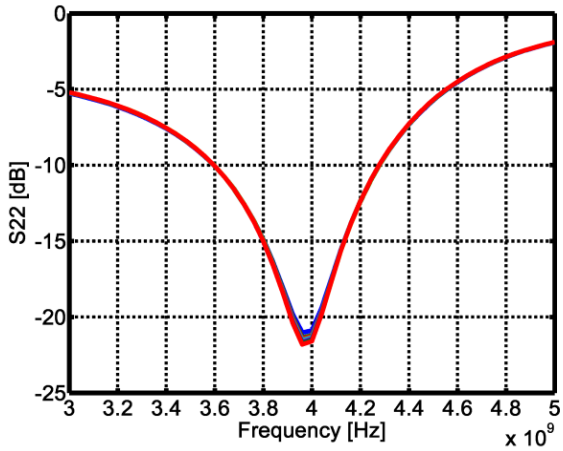

Fig. 8.The Output Return Loss (S_{22}) as a Function of Frequency.The output return loss always remains low at -21.37dB at 4GHz because of the constant biasing current at output stage.

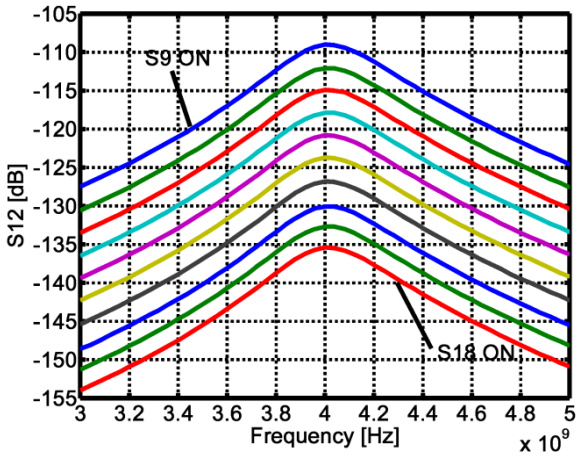

Fig. 9.The Reverse Isolation (S_{12}) as a Function of Frequency

B. Voltage Gain and Power Gain

The variation of the voltage gain as a function of frequency is shown in Fig.10. The gain varies from 15dB (when S_9 is ON) to -12dB (when S_{18} is ON) in 3dB steps with a center frequency of 4GHz. A constant bandwidth of 250MHz is maintained over the entire gain variation.

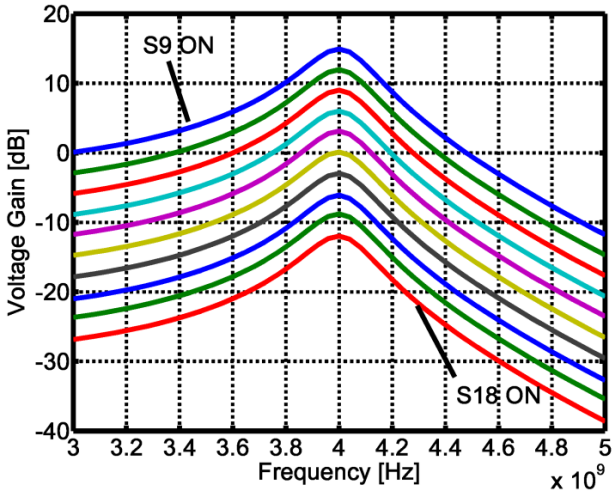

Fig. 10.The Voltage Gain in dB as a Function of Frequency. The gain varies from -12 to 15dB in 3dB steps for a 250MHz bandwidth centered at 4GHz.

The VGA power gain is shown in Fig.11 as a function of frequency. The maximum power gain is 16.17dB(when S_9 is ON) and the minimum power gain is -10.73dB (when S_{18} is ON).The VGA dissipates 5mW of power at the highest gain whileit only dissipates 3.8mW at the lowest gain.

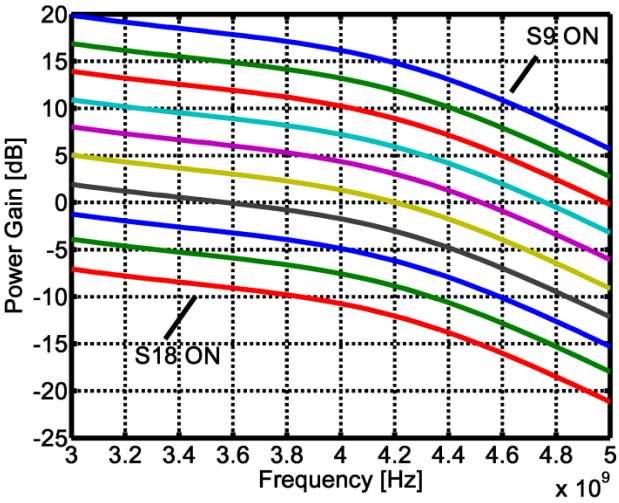

Fig. 11.The Power Gain in dB as a Function of Frequency. The Power Gain Remains Constant Across a 250MHz bandwidth at 4GHz.

C. Noise Figure

The Noise Figure of the VGA is shown in Fig. 12.The minimum noise figure, achieved at a voltage gain of 15dB, is

5.21dB, whereas the highest noise figure, achieved at a voltage gain of -12dB, is 24.6dB. Most noise contributions come from the resistive loss associated with the non-ideal inductors used in the design, especially L_g.

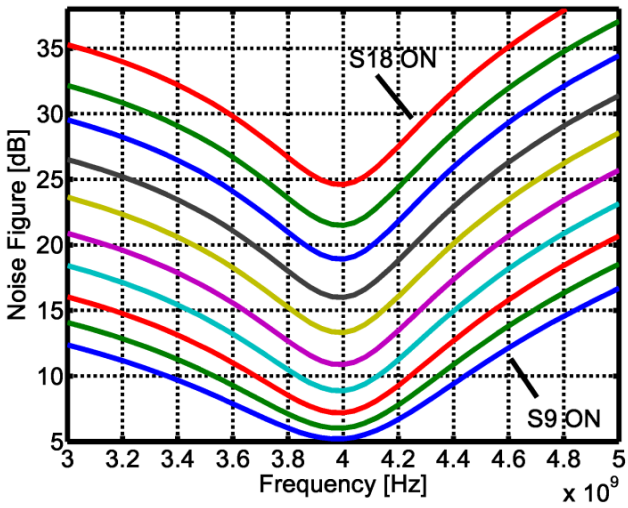

Fig. 12.The Overall Noise Figure as a Function of Frequency. Noise Figure Changes From 5.21dB to 24.6dB for Voltage Gains from 15dB to -12dB.

D. 1_{db} Power Compression Point

The output referred 1_{dB} Power Compression point as a function of gain is represented in Fig. 13. A maximum and minimum Compression point of -18.18dBm and -43dBm is achieved respectively. The figure shows that as the voltage gain of the VGA is decreased the power gain also decreases, indicating that the VGA reaches its saturation power level earlier, hence having a low output referred compression point at lower gains.

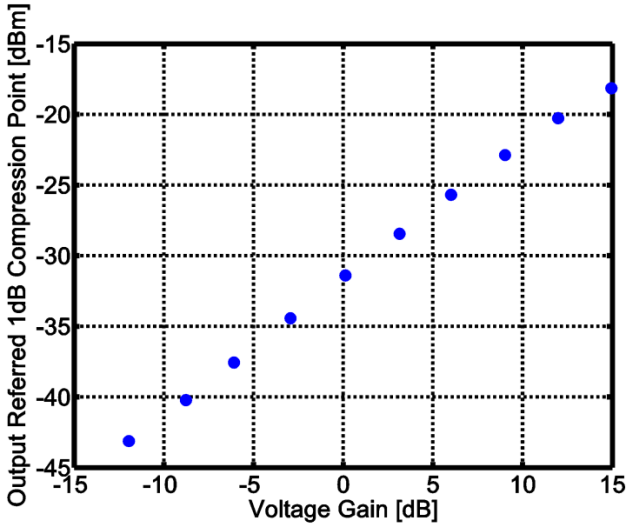

Fig. 13.The Output Referred 1_{dB} Power Compression Point as a Function of Voltage Gain at 4GHz Frequency.

E. Stability

The stability of the VGA can be evaluated by considering the i) Stern Stability Factor K_f and ii) $B_{1f} = s_{11}\, s_{22} - s_{12}\, s_{21}$[11 and 12]. The plots for the log(K_f) and B_{1f}, for different value of gains,are illustrated in Figs. 14 and 15, respectively. Log(K_f) is used instead of regular K_f, because the data were widely spread and a semi log plot better depicts the results. As shown in the graphs,$K_f>1$or Log(K_f)>0 and $B_{1f}>0$ for all gains, indicating that the VGA is always stable.

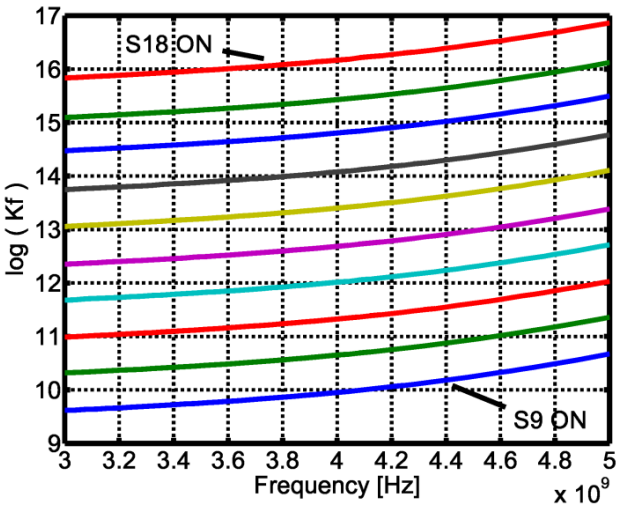

Fig. 14. The Stern Stability Factor,Log(Kf), as a Function of Frequency.

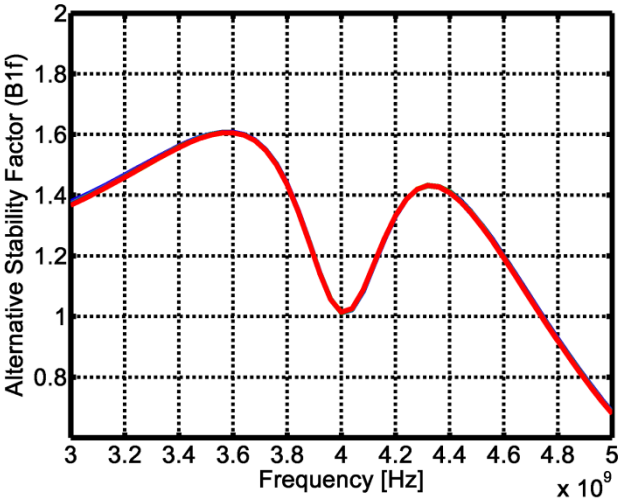

Fig. 15.The B_{1f}Plot as a Function of Frequency for Different Values of Gain.The B1f Remains Greater than 0 Around the Bandwidth of Interest at 4GHz for all Gain Variations.

F. Transient Analysis

To simulate the behavior of the VGA as a function of time, control signals were applied toswitches S_9, S_{10}, S_{11}, …., S_{17} and S_{18} in order to turn a particular stage ON while other current steering stages are turned OFF for a given duration of

time. A sine wave is applied at the input and the corresponding output amplitudeof the VGA verses time, is shown in Fig.16. As can be seen from the figure, different stagesprovide -12dB to 15dB gain in 3dB steps.

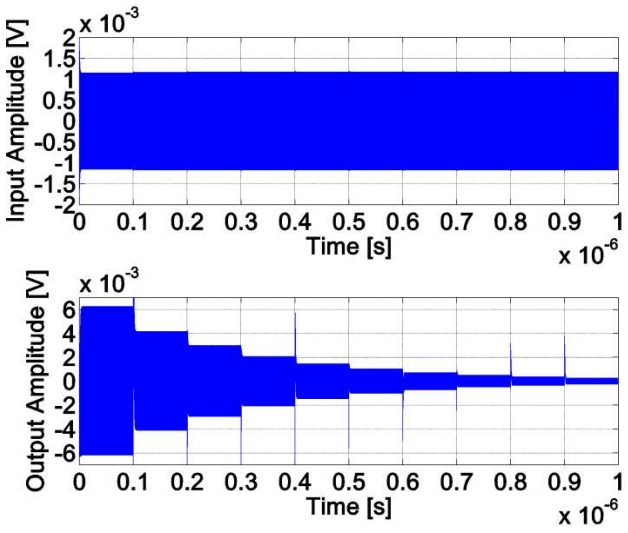

Fig. 16. The Output Transient Response of the VGA for a 4GHz Input Sine Wave

G. Temperature and Processes Variations

Processes variations are minimized by using matched layout techniques and the use of dummy transistors. The temperature of the circuit was swept from -20ºC to 80ºC. The achieved voltage gain verses the expected voltage gain for different values of temperature is shown in Fig. 17. This figure indicates that the maximum positivegain error occurs at 0ºC forall gain stages while the maximumnegative gain error occurs at80ºC for all gain stages. There is approximately 5dB difference between the maximum positive gain error and the maximum negative gain error. The S_{11} and S_{22} versus the voltage gain for different values of temperature are shown in Figs. 18 and 19.

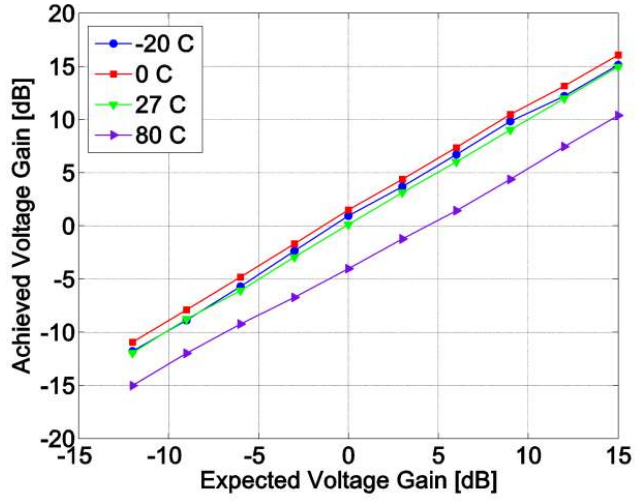

Fig. 17.The Achieved Voltage Gain Verses the Expected Voltage Gain for Different Temperatures

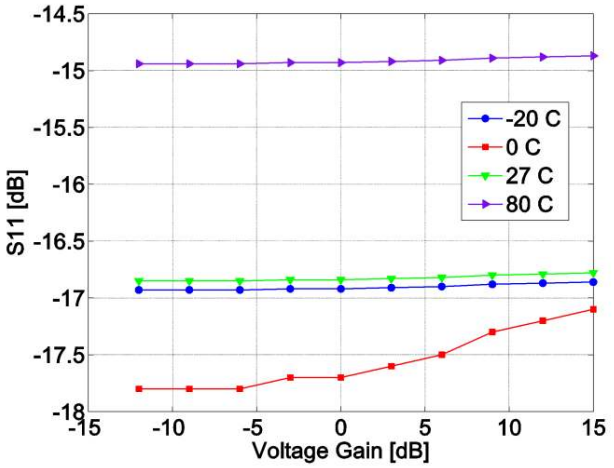

Fig. 18.The S_{11}Versusthe Voltage Gain for Different Temperatures

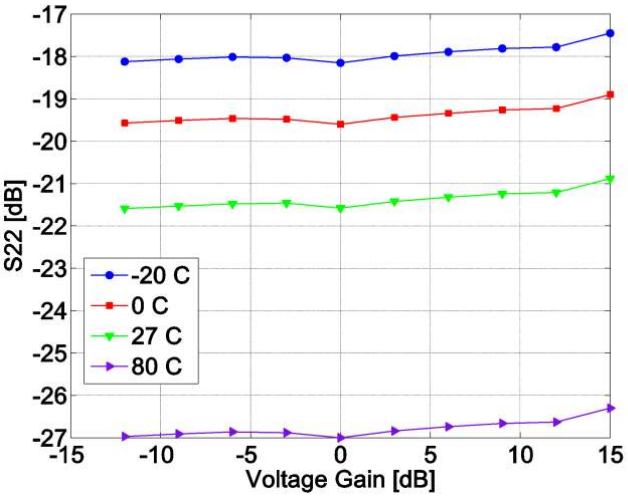

Fig. 19.The S_{22} versus the Voltage Gain for Different Temperatures

The complete VGA characteristics with transistor sizes are summarized in Table 1. The voltage gain of the VGA varies from -12dB to 15dB in 3dB steps with relatively constant input and output return losses of -16.83dB and -21.37dB, respectively. The VGA has a 1dB Power Compression point of -18.15dBm at a voltage gain of 15dB. The overall noise figure of the VGA varies from 5.21dB to 24.6dB while its Power Gain changes from -10.73dB to 16.17dB.

A comparison of the VGA, proposed in this work, compared with other previously reported designs is listed in Table 2. Our results are based on postlayout simulations including all parasitics. The Figure of Merit (FOM) referenced in Table 2 isdefined as

$$FOM = Log\left(\frac{DR \times BW}{|\Delta S_{11}| \times P_{dp} \times NF}\right) \qquad (15)$$

where, DR is the dynamic range equivalent to the difference between maximum gain andthe minimum gain, BW is the bandwidth, $\Delta S_{11}$is the maximum change in S_{11}, $P_{dp}$is thepower dissipation and NF isthe minimum Noise Figure. Compared

with other designs, our architectureyields a near to constant return loss at both input and output.

Table 1. Detailed Characteristics of the VGA

Switch ON	PMOS Transistor Widths (µm)*	NMOS Transistor Widths (µm)*	S_{11} (dB)	S_{22} (dB)	Target Voltage Gain (dB)	Achieved Voltage Gain (dB)	Voltage Gain Error (dB)	Power Gain (dB)	Noise Figure (dB)
S_9	43.20 (M_9)	8.76 (M_{9b})	-16.78	-20.88	15	14.95	-0.05	16.17	5.21
S_{10}	25.68 (M_{10})	5.04 (M_{10b})	-16.79	-21.21	12	11.98	-0.02	13.21	6.04
S_{11}	17.40 (M_{11})	3.48 (M_{11b})	-16.8	-21.24	9	9.02	+0.02	10.25	7.20
S_{12}	11.64 (M_{12})	2.40 (M_{12b})	-16.82	-21.32	6	6.01	+0.01	7.24	8.87
S_{13}	8.04 (M_{13})	1.56 (M_{13b})	-16.83	-21.42	3	3.14	+0.14	4.36	10.88
S_{14}	5.52 (M_{14})	1.08 (M_{14b})	-16.84	-21.58	0	0.12	+0.12	1.34	13.32
S_{15}	3.84 (M_{15})	0.84 (M_{15b})	-16.84	-21.46	-3	-2.94	+0.06	-1.71	15.99
S_{16}	2.64 (M_{16})	0.60 (M_{16b})	-16.85	-21.48	-6	-6.09	-0.09	-4.86	18.92
S_{17}	1.92 (M_{17})	0.36 (M_{17b})	-16.85	-21.53	-9	-8.77	+0.23	-7.54	21.49
S_{18}	1.32 (M_{18})	0.12 (M_{18b})	-16.85	-21.59	-12	-11.95	+0.05	-10.73	24.6

*All transistor Lengths are 100nm.

Table 2.The Comparison of the VGA with Previous Works

Ref.	[6]	[13]	[14]	[15]	[16]	[17]	[18]	This Work
Technology	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.18µm CMOS	0.25µm BiCMOS	0.18µm CMOS	GaAs HBT	0.09µm CMOS
Freq. (GHz)	2.4	5.78	–	–	–	–	–	4
BW (MHz)	41	1000 (MP)	470 to 870	54 to 880	900	50 to 860	1500	250
V_{dd} (V)	1.5	1	1.8	1.8	2.8	1.8	7	1.2
Gain Variation	18.37 (HGM) 6.4 (LGM)	10.11 (HGM) 1.6 (LGM)	16dB to -17dB	15.5 (HGM) -5 (LGM)	28.2 to -21.8	30dB	10dB to 35.6dB	15dB to -12dB
S_{11} (dB)	-12.01 (HGM) -19 (LGM)	-10.69 (HGM) -15 (LGM)	-11 to -26 (MP)	-18 (MGM) -32 (HGM)	-15 to-34	-7 to-16	-5 to-7.5	-16.83
$\lvert\Delta S_{11}\rvert$ (dB)	6.99	4.31	15	14	19	9	2.5	0.07
S_{22} (dB)	-10.53 (HGM) -15.05 (LGM)	–	–	–	-9 to-26	-11 to -16	-5 to-20	-21.37
$\lvert\Delta S_{22}\rvert$ (dB)	4.52	–	–	–	17	5	15	0.71
NF (dB)	2.15 (HGM) 3.97 (LGM)	1.94 (HGM) 3.96 (LGM)	4.3dB to 35dB	3.6 (HGM) 12.2 (LGM)	5 dB at Max Gain	2.5 to 3.5 withNC	2dB to 11dB	5.2 1dB to 24.6dB
P_{1dB} (dBm)	-11.22 (HGM) -9(LGM)	-16 (HGM) -14.5(LGM)	–	–	8.7 Max Gain	–	–	-18.18 to -43
P_{dp} (mW)	6.45	6.4	21.96	50.4	84	19.8	278.6	3.8 to 5
FOM	2.35	3.20	8.89	5.21	15.71	14.44	5.82	23.13

HGM: High Gain Mode, LGM: Low Gain Mode, MP: Measured from Plot, FOM: Figure of Merit

IV. CONCLUSION

This paper presented a novel Variable Gain Amplifier operating at a central frequency of 4GHz with a bandwidth of 250MHz designed in a 90nm CMOS process. The voltage gain of the VGA varies from -12dB to 15dBin 3dB steps. This configuration provides a constant input return loss of -16.83dB and a constant output return loss -21.37dB when gain is varied. The VGA has a 1dB Power Compression point of -18.15dBm at a voltage gain of 15dB. The overall noise figure of the VGA varies from 5.21dB to 24.6dB while its Power Gain changes from -10.73dB to 16.17dB. The design has a very reliable performanceand can be fully integrated forhigh frequency automatic gain control applications.

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